UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,565	11/13/2001	Peter F. Corbett	112056-0015	6718

24267 7590 06/22/2005

CESARI AND MCKENNA, LLP
88 BLACK FALCON AVENUE
BOSTON, MA 02210

EXAMINER	
THAI, HANH B	

ART UNIT	PAPER NUMBER
2161	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,565	CORBETT, PETER F.	
	Examiner	Art Unit	
	Hanh B. Thai	2161	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment field 4/11/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,38,40,41,43,44 and 46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22,38,40,41,43,44 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This is in response to amendment filed April 11, 2005.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment to claims 1-9, 38, 40-41, 43-44 and 46 are acknowledged. Consequently, 35 U. S. C. 101 rejection to the claims is withdrawn.

2. Applicant's arguments on pages 10-12 have been fully considered but they are not persuasive.

Applicant argues that "Burton does not show Applicant's claimed novel step of combining a plurality of unbalanced strip arrays to form the balanced array and distributing assignment of storage devices to parity groups throughout the balanced array." Examiner respectfully disagrees.

Burton discloses the assignment of number of drives corresponding to "unbalanced strip arrays" into a logical array ([0021]), this assignment providing an equal number of disk drives in each span of the array ([0022]) which is considered to be "balanced" array. Therefore, this teaching clearly reads on the claimed limitation of combining a plurality of unbalanced strip arrays to form the balanced array and distributing assignment of storage devices to parity groups throughout the balanced array.

"Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure. In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not read into the claim. > E-Pass Techs., Inc. v. 3Com Corp., 343 F.3d 1364, 1369, 67 USPQ2d

1947, 1950 (Fed. Cir. 2003) (claims must be interpreted "in view of the specification" without importing limitations from the specification into the claims unnecessarily)." (MPEP.2106).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 8-12, 14-22, 38, 40-41, 43-44 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Burton et al. (US Pub. 2003/0074527).

Regarding claim 1, Burton discloses a method for enabling parity declustering in a balanced parity array of a storage system, the method comprising the steps of:

- combining a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks ([0017]; [0018]; [0019]; [0021]-[0025]; [0040]; [0041] and [0043]).
- distributing assignment of storage devices to parity groups throughout the balanced array ([0021]; [0040]; [0043] and [0049]).

Regarding claim 3, Burton does not disclose use the terminology "a filer". But, Burton discloses a storage system that contains the data groups or spans to be assigned to a logical array ([0006]; [0010]; [0017] and [0021]) that corresponds to the filer.

Regarding claim 8, Burton further discloses the steps of configuring the balanced array as a RAID-4 style array; initially under-populating the array with storage devices; and adding

storage devices until a fully populated array of predetermined size is achieved ([0017] and [0026]).

Regarding claim 9, Burton further discloses that the storage devices are disks ([0017]; [0019] and [0021]).

Regarding claim 10, Burton discloses a system that enables parity declustering in a balanced parity array of a storage system, the system comprising:

- a plurality of storage devices, each storage device divided into blocks that are further organized into stripes, wherein each stripe contains data and parity blocks from each of the devices of the balanced array ([0017]; 0018]; [0019] and [0021]-[0025], Burton. Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data);
- a storage operating system (8, Fig.1) including a storage layer configured to implement a parity assignment technique that distributes assignment of devices to parity groups throughout the balanced array ([0040]; [0041]; [0043]; Fig.1-2 and corresponding text, Burton). Please note that "storage system 8" corresponds to the "storage operating system"; and
- a processing element configured to execute the operating system to thereby invoke storage access operations to and from the balanced array in accordance with the concentrated parity technique ([0009]; [0017]; [0040]; [0041]; [0043]; Fig.1-2 and corresponding text, Burton). Please note that the "processor" (10, Fig.1, Burton) corresponds to "a processing element".

Regarding claim 11, Burton discloses the storage layer further combines a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks (([0009]; [0017]; [0040]; [0041]; [0043], Burton).

Regarding claim 12, Burton further discloses the storage devices are disks and wherein the storage layer is a RAID layer ([0018]; [0019] and [0021], Burton).

Regarding claim 14, Burton discloses the storage system is a network-attached storage appliance ([0019]; Fig.1 and corresponding text, Burton).

Regarding claim 15, Burton further discloses that the storage devices are one of video tape, optical, DVD, magnetic tape and bubble memory devices ([0019]; [0046] and [0050], Burton).

Regarding claim 16, Burton further discloses that the storage devices are media adapted to store in formation contained within the data and parity blocks ([0046] and [0050], Burton).

Regarding claims 17 and 20, Burton discloses an apparatus for enabling parity declustering in a balanced parity array of a storage system, the apparatus comprising:

- means for combining a plurality of unbalanced stripe arrays to form the balanced array, each unbalanced stripe array having parity blocks on a set of storage devices that are disjoint from a set of storage devices storing data blocks ([0017]; [0018]; [0019]; [0021]-[0025]; [0040]; [0041] and [0043], Burton); and
- means for distributing assignment of devices to parity groups throughout the balanced array such that all storage devices contain the same amount of data or parity information ([0021]; [0040]; [0043] and [0049], Burton).

Regarding claims 18 and 21, Burton further discloses means for dividing each storage device into blocks; and means for organizing the blocks into stripes across the devices, wherein each stripe contains data and parity blocks from each of the devices of the balanced array ([0017]; 0018]; [0019]; [0021] and [0025]. Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data).

Regarding claims 19 and 22, Burton further discloses the selecting patterns of characters representing data storage devices of a stripe ([0021], Burton).

Regarding claims 38 and 40, Burton discloses a method for declustering a parity array having a plurality of storage devices, the method comprising the steps of:

- assigning a first plurality of data and parity blocks to a first parity group ([0017]; [0018]; [0019] and [0021]-[0025], Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data); and
- assigning a second plurality of data and parity blocks to a second parity group, the first and second parity groups being independent from each other and distributed throughout the plurality of storage devices of the parity array ([0017]; [0018]; [0019]; [0021]; [0025] and Fig.2. Burton shows in Fig.2 that the parity group in span1 is different from span2, span3. Therefore, they are considered being independent from each other).

Regarding claims 41 and 43, Burton discloses a declustered parity array, comprising:

- a plurality of storage devices having a first and second parity group (abstract; [0017]; [0018]; [0019]; [0021]-[0025], Burton);
- a first plurality of data and parity blocks assigned to the first parity group; and a second plurality of data and parity blocks assigned to the second parity group, the first and second parity groups being independent from each other and distributed throughout the plurality of storage devices of the parity array ([0017]; [0018]; [0019]; [0021]; [0025] and Fig.2. Burton shows in Fig.2 that the parity group in span1 is different from span2, span3. Therefore, they are considered being independent from each other).

Regarding claims 44 and 46, Burton discloses a declustered parity array, comprising:

- a plurality of storage devices (abstract; [0017]; [0018]; [0019]; [0021]-[0025], Burton);
- means for assigning a first plurality of data and parity blocks to a first parity group ([0017]; [0018]; [0019] and [0021]-[0025], Burton discloses a computer system include an adaptor to manage the plurality of storage disk drives whereas the storage device is assigned to span and organized into strips contains parity and data); and
- means for assigning a second plurality of data and parity blocks to a second parity group, the first and second parity groups being independent from each other and distributed throughout the plurality of storage devices of the parity array ([0017]; [0018]; [0019]; [0021]-[0025] and Fig.2. Burton shows in Fig.2

that the parity group in span1 is different from span2, span3. Therefore, they are considered being independent from each other).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burton et al. (US Pub. 2003/0074527) in view of Baylor et al. (US Patent no. 5,862,158).

Regarding claim 2, Burton discloses all of the claimed limitations as discussed above except that all surviving data storage devices are loaded uniformly during reconstruction of the failed storage device or devices. Baylor discloses a method for providing fault tolerance against double device failures in multiple device systems including the steps of surviving data storage devices and reconstructing storage device failures (col. 2, lines 28-55 and col.4, line 61 to col.5, line 4, Baylor). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Burton to include the claimed limitation as taught by Baylor. The motivation of doing so would have been to enhance the storage device system's availability.

Regarding claim 4, Burton discloses all of the claimed limitations as discussed above except the steps of dividing each storage device into blocks; and organizing the blocks into stripes across the devices, wherein each stripe contain data and parity blocks from each of the devices of the balanced array. Baylor discloses a method for providing fault tolerance against double device failures in multiple device systems that storage device is divided into multiple data

blocks and organized the blocks into a set of data stripes (col.2, lines 28-55 and col.4, line 61 to col.5, line 4, Baylor). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify Burton to include the claimed limitation as taught by Baylor. The motivation of doing so would have been to enhance the storage device system's availability.

Regarding claim 5, Burton/Baylor combination further discloses the step of selecting patterns of characters representing data storage devices of a stripe to thereby change the association of the data storage devices with parity groups from stripe to stripe of the balanced array (see col.3, lines 28-45; col.4, lines 6-28, Baylor).

Regarding claim 6, Burton/Baylor combination further discloses that the characters are binary numbers (col. 5, lines 1-3, Baylor).

5. Claims 7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burton et al. (US Pub. 2003/0074527) in view of Baylor et al. (US Patent no. 5,862,158) in view of Karr (US Patent no. 3,993,862).

Regarding claim 7, Burton and Baylor combination discloses all of the claimed limitation as discussed above, except "the characters are ternary numbers." Karr, however, discloses a system for compressing source data whereat the characters is ternary numbers (see col.4, lines 4-63, Karr). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Burton and Baylor including the claimed feature as taught by Karr. The motivation of doing so would have been to increase the system's performance and improve memory utilization ([0010], Burton).

Regarding claim 13, Burton/Baylor /Karr discloses the RAID layer is implemented in logic circuitry (see Fig.3-5 and corresponding text, Karr).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jones et al. (US 5,657,439) discloses distributed subsystem sparing.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hanh B. Thai whose telephone number is 571-272-4029. The examiner can normally be reached on 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Safet Metjahic can be reached on 571-272-4023. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hanh B Thai
Examiner
Art Unit 2161

June 10, 2005

UYEN LE
PRIMARY EXAMINER